IN THE SPECIFICATION

Please amend the first paragraph on page 1, lines 4-9 as follows:

The present invention relates to a distortion compensating apparatus and, more particularly, to a distortion compensating apparatus ~~having a function of obtaining the delay time caused generated in a power amplifier and a feedback loop~~ for compensating for a distortion of a transmission power amplifier, using the correlation between a transmission signal and a feedback signal, and adjusting a timing of each element of the distortion compensating apparatus on the basis of ~~the~~ a delay time obtained.

Please amend the paragraph starting on page 1, line 19 and ending on page 2, line 8 as follows:

FIG. 23 is a block diagram of an example of a transmitter in a conventional radio apparatus. A transmission signal generator 1 sends a group of serial digital data, and a serial/parallel (S/P) converter 2 alternately separates the group of digital data bit by bit into an in-phase component (I) signal and a quadrature component (Q) signal. A ~~DA~~ D/A converter 3 converts each of the I signals and Q signals into analog baseband signals and inputs the base band signals into a quadrature modulator 4. The quadrature modulator 4 multiplies the input I and Q signals (transmission baseband signals) by a reference carrier wave and signal phase-shifted from the reference carrier by 90°, respectively, adds the two products, thereby performing a quadrature conversion, and outputs the result. A frequency converter 5 mixes the signal subjected to quadrature modulation and a local oscillation signal to perform a frequency conversion, and a transmission power amplifier 6 amplifiers the power of the carrier wave output by the frequency converter 5 and radiates the amplified signal into space from an antenna 7.

Please amend the paragraph on page 12, lines 4-15 as follows:

FIG. 1 is a schematic explanatory view of a first present invention. In FIG. 1, the reference numeral 51a denotes a pre-distortion unit for multiplying a transmission signal x(t) by a distortion compensation coefficient $h_n(p)$ (actually a complex number), 51b a ~~DA~~ D/A converter, 51c a device (e.g., transmission power amplifier) in which a distortion generates, 51d a feedback system, 51e an ~~AD~~ A/D converter, 51f a distortion compensation coefficient memory for storing the distortion compensation coefficient $h_n(p)$ corresponding to the power p of a transmission signal x(t), 51g an arithmetic unit for calculating the power p of a transmission signal (x)t, 51h a delay circuit for generating a writing address, and 51i a distortion compensation coefficient arithmetic unit for calculating a distortion compensation coefficient by an adaptive algorithm using the LMS (Least Means Square) method.

Please amend the paragraph on page 13, lines 1-11 as follows:

A delay time decision unit 71 calculates the correlation between a transmission signal x(t) before a distortion compensation processing and a feedback signal, decides the total delay time ($D_0 + D_1$) caused in the transmission power amplifier 51c, the feedback system ~~51e~~ 51d, etc. on the basis of the maximum correlation, and sets the total delay time in each of the delay circuits 51h, 61b and 61g. That is, attention is paid to the correlation between a transmission signal x(t) and a feedback signal, both signals are input to a correlator 71a, the correlation obtained by adjusting time difference between both signals is monitored, and the timed difference at which the correlation is the maximum is set as the total amount of delay due to the transmission power amplifier and a device in the feedback loop, thereby compensating for a distortion.

Please amend the paragraph on page 33, lines 4-17 as follows:

FIG. 15 shows the structure of a fourth embodiment of a delay time decision unit for deciding the delay time with high precision. The same reference numerals are provided for the elements which are the same as those in the first embodiment. The fourth embodiment is different from the first embodiment in that the delay unit 81 is constituted by a clock phase variable circuit for varying the phase of the sampling clock of the ~~AD~~ A/D converter 51e. More specifically, the delay unit 81 is provided with a sampling clock generator CLG, and a clock phase delay element CDE for varying the clock phase by ΔD. If there is a need for increasing the amount of delay by ΔD at step 2004 in FIG. 11, the delay time decision unit 71 inputs a clock phase changing signal CPC into the delay unit 81. When the delay unit 81 receives the clock phase changing signal CPC, it increases the phase of the sampling clock by ΔD, and inputs the sampling clock into the ~~AD~~ A/D converter 51e. As a result, the sampling timing increases by ΔD, and the delay time increases by that amount.

Please amend the paragraph on page 36, lines 15-20 as follows:

The DLL circuit 91 in the example shown in FIG. 16 has the structure framed by the dotted line in FIG. 17. In this example, a transmission signal output from the delay circuit 61b is used in place of the PN sequence A, a feedback signal output from the ~~AD~~ A/D converter 51e is used in place of the received signal train B, and the output C of the filter 91f is input into the delay unit 81.

Please amend the paragraph starting on page 36, line 21 and ending on page 37, line 3 as follows:

As explained above, in the example shown in FIG. 16, the delay time D and the amount Dv of delay are calculated in the state in which the DLL circuit 91 is turned off, in the method explained with reference to FIGS. 10 and 11, and these results are set in each of the delay circuits 51h, 61b and 61g, and the delay unit 81. Thereafter, when the DLL circuit 91 is activated, it shows the characteristic shown in (c) of FIG. 18 with respect to the phase difference between the transmission signal A output from the delay circuit 61b and the feedback signal B output from the ~~AD~~ A/D converter 51e, controls the clock frequency such that the error is zero, and outputs the delay control signal C.

Please amend the paragraph on page 40, lines 14-20 as follows:

At the time of training, the training data generator 62 generates known training data T_0, T_1, T_2, ...Tn, and the switch 63 selects the training data r(t) and inputs them into the distortion compensating apparatus. The switch 64 is turned on, and the feedback data output from the ~~AD~~ A/D converter 51e are input into the matched filter 71a of the delay time decision unit 71, which shifts the data to a shift register SFR and stores them.